Electronic Version
Stylesheet Version v1.1.1

[STACK-GATE FLASH MEMORY ARRAY]

Abstract

The present invention provides a stack-gate flash memory array. In the present invention, one bit line for a conventional memory cell had been divided two independent bit lines; two word lines have been combined together via the gate terminal of an isolated transistor. Because the bit lines are divided and the word lines will stop the leakage current via the isolated transistor, the leakage current would not affect the other memory cells. Hence, the present invention can avoid the data inaccuracy due to the leakage current resulting from the erratic bits, and thus can extend the flash memory's lifetime.